

CD4019B Types

CMOS Quad AND/OR Select Gate

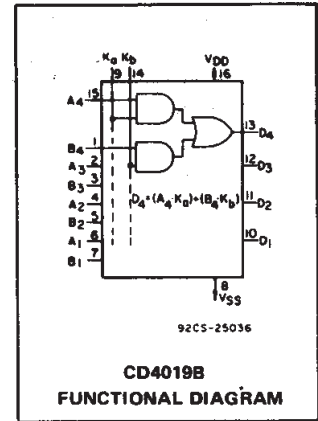
High-Voltage Types (20-Volt Rating)

■ CD4019B types consist of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_A and K_B . In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical $A + B$ function.

The CD4019B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- Medium-speed operation
... $t_{PHL} = t_{PLH} = 60$ ns (typ.) at $C_L = 50$ pF, $V_{DD} = 10$ V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
 1 V at $V_{DD} = 5$ V
 2 V at $V_{DD} = 10$ V
 2.5 V at $V_{DD} = 15$ V



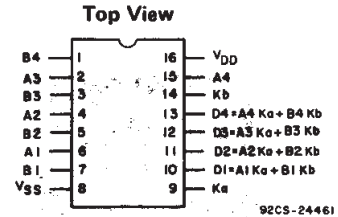
MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})		-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS		-0.5V to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT		± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):		
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$		500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$		Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)		100mW
OPERATING-TEMPERATURE RANGE (T_A)		-55°C to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})		-65°C to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10s max		$+265^\circ\text{C}$

Applications:

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/Exclusive-OR selection

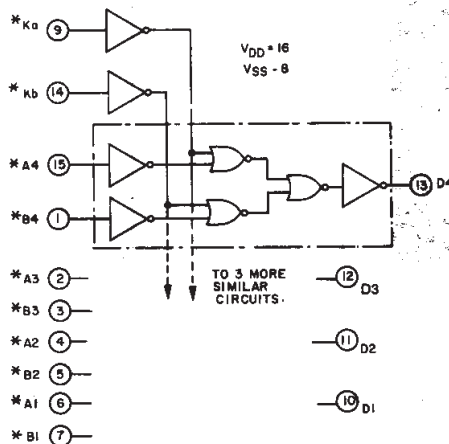
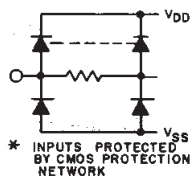
TERMINAL DIAGRAM



TRUTH TABLE

K_A	K_B	A_n	B_n	D_n
1	0	1	X	1
1	0	0	X	0
0	1	X	1	1
0	1	X	0	0
0	0	X	X	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

X = Don't Care



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	Min.	Max.	Units
Supply Voltage Range (For $T_A =$ Full Package Temperature Range)		3	18	V

Fig. 1—Logic diagram.

CD4019B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0,5	5	1	1	30	30	-	0,02	1	μA
	-	0,10	10	2	2	60	60	-	0,02	2	
	-	0,15	15	4	4	120	120	-	0,02	4	
	-	0,20	20	20	20	600	600	-	0,04	20	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5			0,05			0	0,05	V
	-	0,10	10			0,05				0,05	
	-	0,15	15			0,05				0,05	
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5			4,95		4,95	5	-	V
	-	0,10	10			9,95		9,95	10	-	
	-	0,15	15			14,95		14,95	15	-	
Input Low Voltage, V _{IL} Max.	0,5,4,5	-	5			1,5				1,5	V
	1,9	-	10			3				3	
	1,5,13,5	-	15			4				4	
Input High Voltage, V _{IH} Min.	0,5,4,5	-	5			3,5		3,5		-	V
	1,9	-	10			7		7		-	
	1,5,13,5	-	15			11		11		-	
Input Current I _{IN} Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 ⁻⁵	±0,1	μA

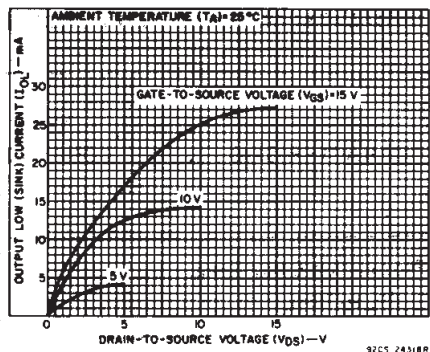


Fig. 2 - Typical output low (sink) current characteristics.

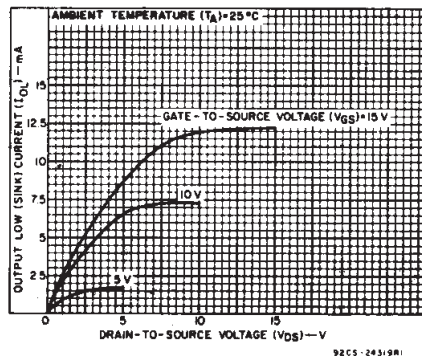


Fig. 3 - Minimum output low (sink) current characteristics.

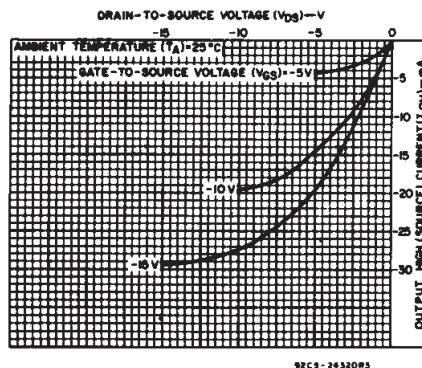


Fig. 4 - Typical output high (source) current characteristics.

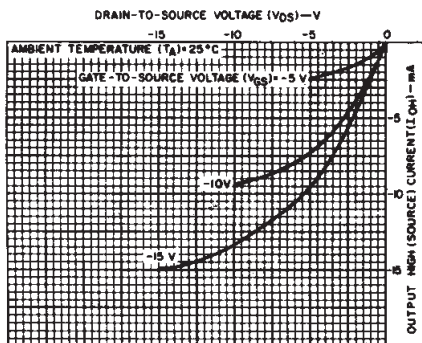


Fig. 5 - Minimum output high (source) current characteristics.

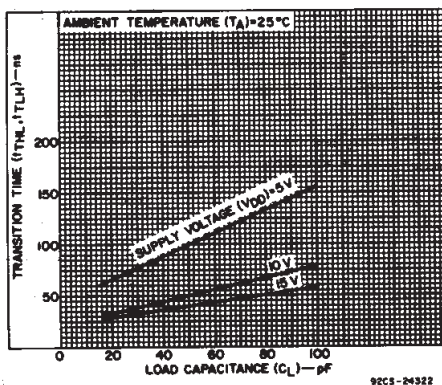


Fig. 6 - Typical transition time as a function of load capacitance.

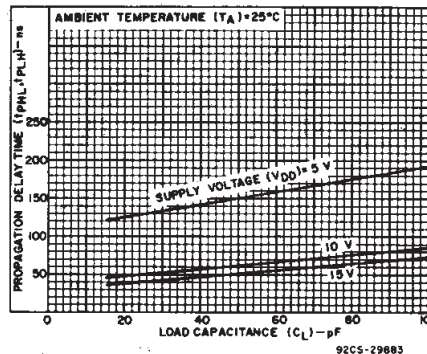


Fig. 7 - Propagation delay time as a function of load capacitance.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4019B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		VDD (V)	Min.	Typ.		Max.
Propagation Delay Time; t_{PLH}, t_{PHL}		5	—	150	300	ns
		10	—	60	120	
		15	—	50	100	
Transition Time; t_{THL}, t_{TLH}		5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Input Capacitance, C_{IN}	All A and B Inputs	—	5	7.5	pF	
	K_a and K_b Inputs	—	10	15	pF	

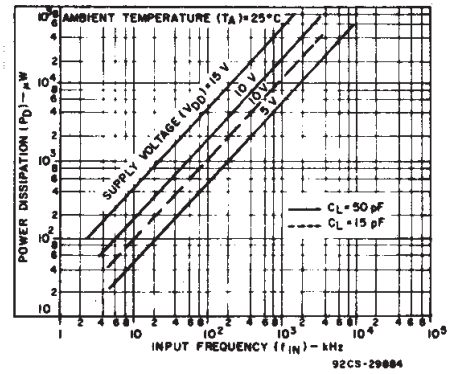


Fig. 8 – Typical dynamic power dissipation as a function of input frequency.

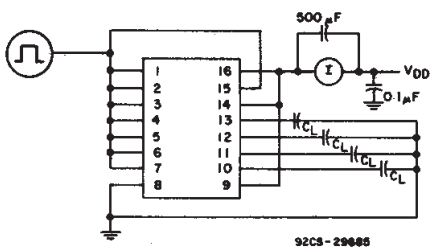


Fig. 9 – Dynamic power dissipation test circuit.

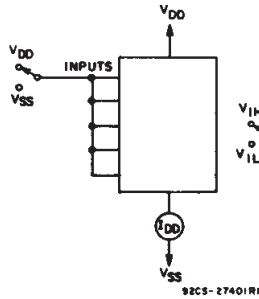


Fig. 10 – Quiescent device current test circuit.

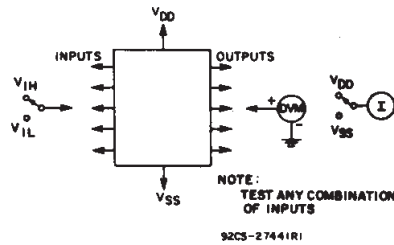


Fig. 11 – Input voltage test circuit.

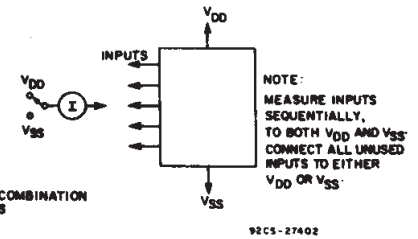


Fig. 12 – Input current test circuit.

TYPICAL APPLICATIONS

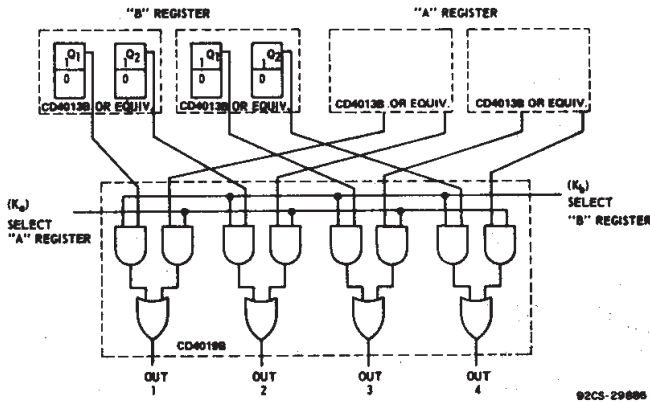


Fig. 13 – AND/OR select gating.

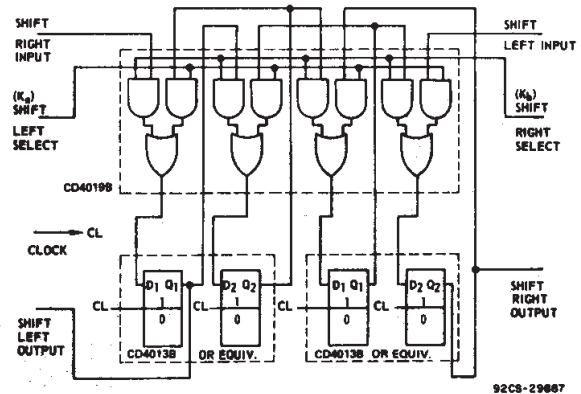


Fig. 14 – "Shift left/shift right" register.

CD4019B Types

TYPICAL APPLICATIONS (CONT'D)

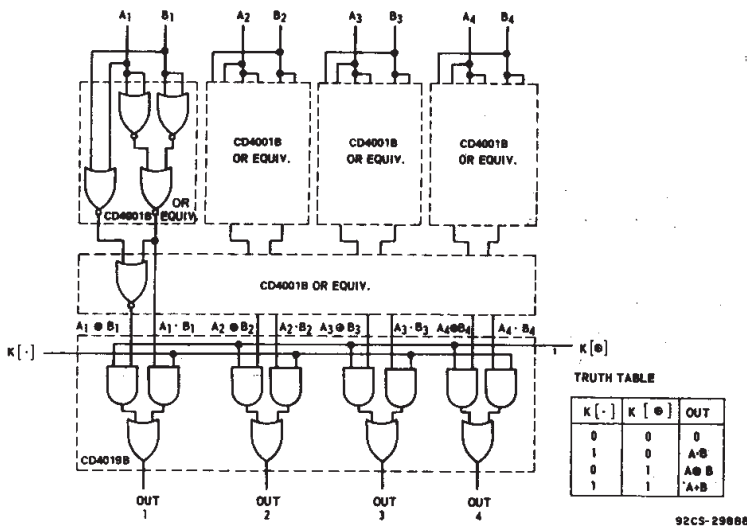


Fig. 15 - AND/OR Exclusive-OR selector.

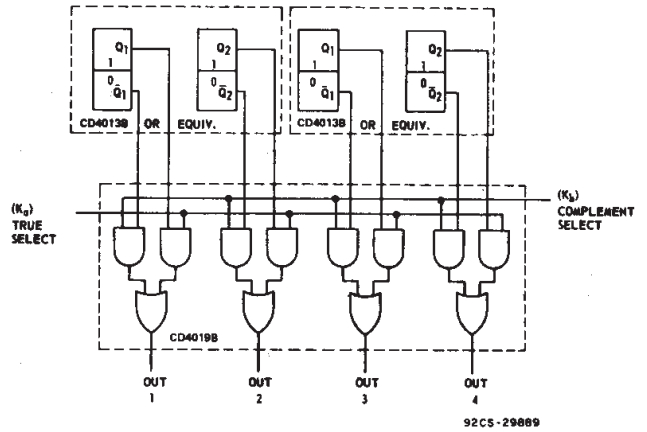
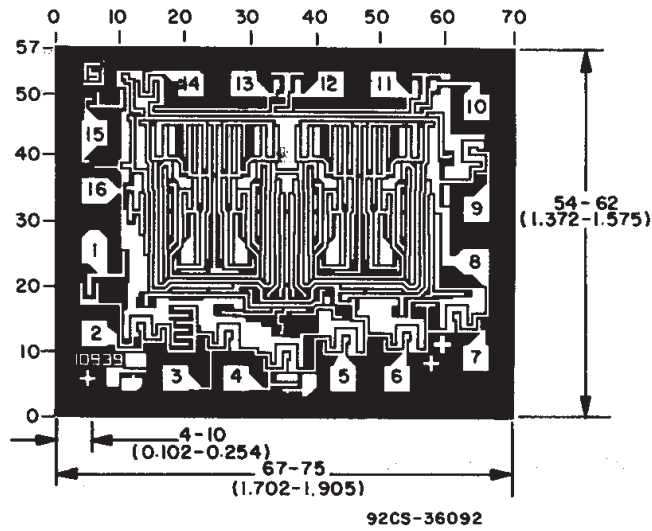


Fig. 16 - "True complement" selector.



Dimensions and pad layout for CD4019BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.